

Serial No: 10/756,961

Examiner: Pham H.

Title: Semiconductor Memory Device With Trench-Type Stacked Cell Capacitors And Method For Manufacturing The Same

REMARKS/ARGUMENTS

Reconsideration is requested in view of the above amendments and the following remarks.

Support for the revision of claim 7 is found in the specification from page 17, line 26 to page 18, line 35, in Figures 6A-6D, and from page 10, line 37 to page 11, line 3.

Support for new claims 16-20 is found in the specification from page 22, line 15 to page 23, line 6.

Support for new claim 21 is found in the specification on page 18, lines 30-35.

Rejections under 35 USC §112

Claim 8 is rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement, particularly for the limitation “a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film”.

Applicant respectfully traverses this rejection.

Exemplary embodiments described on page 22, lines 15-36 of the specification clearly disclose the features of claim 8.

For at least these reasons, claim 8 is enabled.

Claims 7-8 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Applicant respectfully traverses this rejection. The editorial revisions made above overcome the constructive criticisms noted in the rejection.

Claim Rejections -35 USC §102

Claim 7 is rejected under 35 U.S.C. §102(b) as being anticipated by Applicant's Admitted Prior Art (fig. 17).

Applicant respectfully traverses this rejection.

The rejection states in part “Applicant Admitted Prior Art (page 3, fig. 17) discloses a method for manufacturing a semiconductor memory device comprising: patterning a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged so that the adjacent hole patterns are opposite to each other”.

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Claim 7 however, recites patterning a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged in a staggered manner so that side edges of the adjacent hole patterns are only partially opposite to each other.

For at least these reasons, claim 7 is patentable over Applicant's Admitted Prior Art (fig. 17).

Favorable reconsideration in the form of a Notice of Allowance is requested. If the Examiner believes a telephone conference would advance the prosecution of this application, the Examiner is invited to telephone the undersigned at the below-listed telephone number.



Dated: October 5, 2005

Respectfully submitted,

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